WHAT IS CLAIMED IS:

1. An output buffer circuit comprising:

an input terminal for receiving an input signal;

an output terminal for outputting an output signal;

a first inverter connected to the input terminal, the first inverter outputting a first signal having a slow rise up and fall down characteristic;

a second inverter connected to the input terminal, the first inverter outputting a second signal having the slow rise up and fall down characteristic;

a pull up control circuit connected to the input terminal and the output terminal, the pull up control circuit pulling up an output voltage of the first signal when the first signal has a level lower than a first threshold voltage level and stopping the pull up of the output voltage of the first signal when the level of the first signal exceeds the first threshold voltage level;

a pull down control circuit connected to the input terminal and the output terminal, the pull down control circuit pulling down an output voltage of the second signal when the second signal has a level higher than a second threshold voltage level and stopping the pull down of the output voltage of the second signal when the level of the second signal becomes lower than the second threshold voltage level;

a first output transistor having a source connected

to a first power source potential node, a drain connected to the output terminal and a gate connected to the first inverter so as to receive the first signal; and

a second output transistor having a source connected to a second power source potential node, a drain connected to the output terminal and a gate connected to the second inverter so as to receive the second signal.

2. An output buffer circuit according to claim 1, wherein each of the first and second inverters comprises,

an inverter input terminal;

an inverter output terminal;

a first inverter transistor of a first conductivity type having a back gate connected to the second power source potential node, a first terminal, and a second terminal and a gate connected together with the first power source potential node;

a second inverter transistor of a second conductivity type having a back gate connected to the first power source potential node; a first terminal connected to the first terminal of the first inverter transistor, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal;

a third inverter transistor of the second conductivity type having a back gate connected to the first power source potential node, a first terminal, and a second terminal and a gate connected together with the second power source potential node; and

a fourth inverter transistor of the first conductivity type having a back gate connected to the second power source potential node; a first terminal connected to the first terminal of the third inverter transistor, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal.

3. An output buffer circuit according to claim 1, wherein each of the first and second inverter comprises,

an inverter input terminal;

an inverter output terminal;

a first inverter transistor of a first conductivity type having a back gate connected to the first power source potential node, a first terminal, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal;

a first diode connected between the first power source potential node and the first terminal of the first inverter transistor for falling down a voltage supplied from the first power source potential node;

a second inverter transistor of a second conductivity type having a back gate connected to the second power source potential node, a first terminal, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal; and

a second diode connected between the second power source potential node and the first terminal of the second inverter transistor for falling down a voltage supplied from

the first terminal of the second inverter transistor.

4. An output buffer circuit according to claim 3, wherein the first diode having an anode connected to the first power source potential node, and a cathode connected to the first terminal of the first inverter transistor, and wherein the second diode having a cathode connected to the second power source potential node, and an anode connected to the first terminal of the second inverter transistor.

5. An output buffer circuit according to claim 1, wherein the pull up control circuit includes,

a gate circuit having a first input terminal connected to the input terminal of the output buffer circuit, a second input terminal connected to the output terminal of the output buffer circuit and an output terminal, and

a pull up transistor having a first terminal connected to the first power source potential node, a second terminal connected to the inverter output terminal of the first inverter and a gate connected to the output terminal of the gate circuit.

6. An output buffer circuit according to claim 5, wherein the gate circuit is a NAND circuit.

7. An output buffer circuit according to claim 1, wherein the pull down control circuit includes,

a gate circuit having a first input terminal connected to the input terminal of the output buffer circuit, a second input terminal connected to the output terminal of the output buffer circuit and an output terminal, and

a pull down transistor having a first terminal connected to the second power source potential node, a second terminal connected to the inverter output terminal of the second inverter and a gate connected to the output terminal of the gate circuit.

8. An output buffer circuit according to claim 7, wherein the gate circuit is a NOR circuit.

9. An output buffer circuit according to claim 1, further comprising an enable gate circuit having a first input terminal connected to the input terminal of the output buffer circuit, a second input terminal connected to receive an enable signal and a pair of output terminals connected to the inverter input terminals of the first and second inverters, respectively.

10. An output buffer circuit according to claim 9, wherein the enable gate circuit includes,

an AND circuit having a first input terminal connected to the first input terminal of the enable gate circuit, a second input terminal connected to receive the enable signal and an output terminal connected to the inverter input terminal of the first inverter,

a third inverter having an input terminal connected to receive the enable signal and output terminal, and

an OR circuit having a first input terminal connected to the first input terminal of the enable gate circuit, a second input terminal connected to the output terminal of the third inverter and an output terminal

connected to the inverter input terminal of the second inverter.

11. An output buffer circuit comprising:

an input terminal for receiving an input signal;

an output terminal for outputting an output signal;

a first inverter connected to the input terminal, the first inverter outputting a first signal having a slow rise up and fall down characteristic;

a second inverter connected to the input terminal, the first inverter outputting a second signal having the slow rise up and fall down characteristic;

a pull up control circuit connected to the input terminal, the pull up control circuit pulling up an output voltage of the first signal during a predetermined time from a time when the input signal is changed from "L" level to "H" level;

a pull down control circuit connected to the input terminal, the pull down control circuit pulling down an output voltage of the second signal during a predetermined time from a time when the input signal is changed from "H" level to "L" level;

a first output transistor having a source connected to a first power source potential node, a drain connected to the output terminal and a gate connected to the first inverter so as to receive the first signal; and

a second output transistor having a source connected to a second power source potential node, a drain connected to

the output terminal and a gate connected to the second inverter so as to receive the second signal.

12. An output buffer circuit according to claim 11, wherein each of the first and second inverters comprises,

an inverter input terminal;

an inverter output terminal;

a first inverter transistor of a first conductivity type having a back gate connected to the second power source potential node, a first terminal, and a second terminal and a gate connected together with the first power source potential node;

a second inverter transistor of a second conductivity type having a back gate connected to the first power source potential node; a first terminal connected to the first terminal of the first inverter transistor, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal;

a third inverter transistor of the second conductivity type having a back gate connected to the first power source potential node, a first terminal, and a second terminal and a gate connected together with the second power source potential node; and

a fourth inverter transistor of the first conductivity type having a back gate connected to the second power source potential node; a first terminal connected to the first terminal of the third inverter transistor, a second terminal connected to the inverter output terminal and a gate

connected to the inverter input terminal.

13. An output buffer circuit according to claim 11, wherein each of the first and second inverter comprises,

an inverter input terminal;

an inverter output terminal;

a first inverter transistor of a first conductivity type having a back gate connected to the first power source potential node, a first terminal, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal;

a first diode connected between the first power source potential node and the first terminal of the first inverter transistor for falling down a voltage supplied from the first power source potential node;

a second inverter transistor of a second conductivity type having a back gate connected to the second power source potential node, a first terminal, a second terminal connected to the inverter output terminal and a gate connected to the inverter input terminal; and

a second diode connected between the second power source potential node and the first terminal of the second inverter transistor for falling down a voltage supplied from the first terminal of the second inverter transistor.

14. An output buffer circuit according to claim 13, wherein the first diode having an anode connected to the first power source potential node, and a cathode connected to the first terminal of the first inverter transistor, and

wherein the second diode having a cathode connected to the second power source potential node, and an anode connected to the first terminal of the second inverter transistor.

15. An output buffer circuit according to claim 11, wherein the pull up control circuit includes,

a delay circuit having an input terminal connected to the input terminal of the output buffer circuit and an output terminal, and

a pull up transistor having a first terminal connected to the first power source potential node, a second terminal connected to the inverter output terminal of the first inverter and a gate connected to the output terminal of the delay circuit.

16. An output buffer circuit according to claim 11, wherein the pull down control circuit includes,

a delay circuit having an input terminal connected to the input terminal of the output buffer circuit and an output terminal, and

a pull down transistor having a first terminal connected to the second power source potential node, a second terminal connected to the inverter output terminal of the second inverter and a gate connected to the output terminal of the delay circuit.

17. An output buffer circuit according to claim 11, further comprising an enable gate circuit having a first input terminal connected to the input terminal of the output buffer circuit, a second input terminal connected to receive

an enable signal and a pair of output terminals connected to the inverter input terminals of the first and second inverters, respectively.

18. An output buffer circuit according to claim 17, wherein the enable gate circuit includes,

an AND circuit having a first input terminal connected to the first input terminal of the enable gate circuit, a second input terminal connected to receive the enable signal and an output terminal connected to the inverter input terminal of the first inverter,

a third inverter having an input terminal connected to receive the enable signal and output terminal, and

an OR circuit having a first input terminal connected to the first input terminal of the enable gate circuit, a second input terminal connected to the output terminal of the third inverter and an output terminal connected to the inverter input terminal of the second inverter.

19. An output buffer circuit comprising:

an input terminal for receiving an input signal;

an output terminal for outputting an output signal;

a high level control circuit connected to the input terminal, the high control circuit outputting a signal having a level gradually changing from "H" level to "L" level when the input signal is changed from "L" level to "H" level;

a low level control circuit connected to the input terminal, the low control circuit outputting a signal having

a level gradually changing from "L" level to "H" level when the input signal is changed from "H" level to "L" level;

a first output transistor having a source connected to a first power source potential node, a drain connected to the output terminal and a gate connected to the high level control circuit; and

a second output transistor having a source connected to a second power source potential node, a drain connected to the output terminal and a gate connected to the low level control circuit.

20. An output buffer circuit according to claim 19, wherein each of the high level and low level control circuits has an inverter connected to the input terminal, the inverter outputting a signal having a slow rise up and fall down characteristic.